ABSTRACT

A system wherein data is read from, and store in, a memory, such data having associated therewith an address/control portion. The system includes a pair of controller sections, one of such sections being a primary section and the other one of the sections being a secondary section. Both such sections are configured to implement identical control logic in controlling the transfer of such data between a first port connected to the pair of control sections and a write data port. The write data port of the primary section is connected to the memory. The first port receives an address/control portion associated with the data. A checker is included for producing a no-operation (NOOP) command to the memory if logic signal produced by the pair of control logic from the address/control portion at the first port are different from one another. The memory is configured to inhibit storage of data in the memory at the data port in response to the NOOP command.